IN THE CLAIMS

1-5. (Canceled)

6. (Withdrawn) A method for manufacturing a nonvolatile semiconductor memory device comprising:

forming a first gate electrode, which has a first gate length, on a peripheral circuit portion of a semiconductor substrate and a second gate electrode, which has a second gate length shorter than the first gate length, on a memory cell portion of the semiconductor substrate;

introducing impurity into the peripheral circuit portion and memory cell portion with at least the first and second gate electrodes used as a mask;

forming a first insulating film above at least the memory cell portion, the first insulating film covering the second transistors and having a property which makes it difficult for an oxidizing agent to pass therethrough; and

annealing the semiconductor substrate into which the impurity has been introduced in an oxidation atmosphere to diffuse the impurity into the semi-conductor substrate, whereby a first transistor having the first gate electrode and source and drain diffusion layers containing the diffused impurity is formed in the peripheral circuit portion and a second transistor having the second gate electrode and source and drain diffusion layers containing the diffused impurity is formed in the memory cell portion.

7. (Withdrawn) The method for manufacturing the nonvolatile semiconductor memory device according to claim 6, wherein at least the second gate electrode is formed by a method including steps of forming a gate insulating film on the semiconductor substrate,

forming a floating gate on the gate insulating film, forming an inter-gate insulating film on the floating gate and forming a control gate on the inter-gate insulating film.

8. (Withdrawn) The method for manufacturing the nonvolatile semiconductor memory device according to claim 6, further comprising:

forming a second insulating film which is different from the first insulating film and formed between at least the second transistors and the first insulating film.

9. (Withdrawn) The method for manufacturing the nonvolatile semiconductor memory device according to claim 6, further comprising:

forming an inter-level insulating film above the semiconductor substrate after annealing the semiconductor substrate;

forming a first contact hole reaching the first insulating film in the inter-level insulating film; and

etching a part of the first insulating film which are exposed to the bottoms of the first contact hole and forming a second contact hole reaching a source/drain diffusion region of the second transistor in the first insulating film.

10. (Withdrawn) The method for manufacturing the nonvolatile semiconductor memory device according to claim 6, further comprising;

subjecting the surfaces of the first and second gate electrodes to an oxidation process.

11-14. (Canceled)

15. (Withdrawn) A method for manufacturing a nonvolatile semiconductor memory device:

forming a transistor in a memory cell portion of a semiconductor substrate;

covering the transistor with a silicon nitride film; and

subjecting the surface of the silicon nitride film to an oxidation process.

16. (Withdrawn) The method for manufacturing the nonvolatile semiconductor memory device according to claim 15, further comprising:

forming an inter-level insulating film on the semiconductor substrate after subjecting the surface of the silicon nitride film to an oxidation process.

17. (Withdrawn) The method for manufacturing the nonvolatile semiconductor memory device, according to claim 15, wherein the surface of the silicon nitride film is oxidized by a method selected from the group consisting of pyrogenic oxidation and water-vapor oxygen oxidation.

18. (Withdrawn) The method for manufacturing the nonvolatile semiconductor memory device, according to claim 16, wherein the surface of the silicon nitride film is oxidized by a method selected from the group consisting of pyrogenic oxidation and water-vapor oxygen oxidation.

19-25. (Canceled)

26. (Currently Amended) A nonvolatile semiconductor memory device, comprising:

a semiconductor substrate having a peripheral circuit region and a memory cell region;

a first element region provided in the ~~peripheral circuit~~ memory cell region;

a second element region provided in the ~~memory cell~~ peripheral circuit region;

~~a first element isolation region provided in the semiconductor substrate, the first element isolation region isolating the first element region;~~

~~a second element isolation region provided in the semiconductor substrate, the second element isolation region isolating the second element region;~~

a ~~first transistor~~ memory cell having source and drain diffusion layers each provided in the first element region;

a ~~second~~ peripheral transistor having source and drain diffusion layers each provided in the second element region; ~~and~~

an element isolation region being in contact with the first element region;

an insulating film covering ~~the first and second transistors~~ the memory cell, the peripheral transistor, and the element isolation region, and containing an insulator different from the element isolation region, the insulating film being harder for an oxidizing agent to pass therethrough, compared with a silicon oxide film, and a surface of the insulating film being oxidized;

an inter-level insulating film provided on the surface of the insulating film, the inter-level insulating film containing an insulator different from the insulating film;

a contact hole provided in the inter-level insulating film and the insulating film, the contact hole reaching at least one of the source and drain diffusion layers of the memory cell and overlapping the element isolation region; and

a contact plug provided in the contact hole, the contact plug being in contact with at least one of the source and drain diffusion layers of the memory cell, the insulating film, and the inter-level insulating film.

27. (Currently Amended) The device according to claim 26, wherein surfaces of gate electrodes of ~~the first and second transistors~~ the memory cell and the peripheral transistor are oxidized.

28. (Previously Presented) The device according to claim 26, wherein the insulating film has a thickness of at most 50 nm.

29. (Previously Presented) The device according to claim 26, wherein the insulating film includes a silicon nitride film.

30. (Previously Presented) The device according to claim 29, wherein a surface of the silicon nitride film is oxidized.

31. (Previously Presented) The device according to claim 30, wherein a thickness of an oxidized region of the silicon nitride film is at least 1 nm and at most 10 nm.

32. (Previously Presented) The device according to claim 29, wherein the silicon nitride film contains hydrogen, and a concentration of the hydrogen is at most $3 \times 10^{21}$ atom/cm$^3$.

33. (Previously Presented) The device according to claim 29, wherein the silicon nitride film contains hydrogen, and a concentration of the hydrogen gradually becomes higher from the surface of the silicon nitride film.

34. (Currently Amended) The device according to claim 26, wherein a gate electrode of each of the ~~first~~ memory cell and ~~second transistors~~ the peripheral transistor contains a metal or a metal silicide.

35. (Previously Presented) The device according to claim 34, wherein the metal contains tungsten.

36. (Currently Amended) The device according to claim 26, wherein a gate electrode of each of the ~~first and second transistors~~ memory cell and the peripheral transistor is a stacked gate structure including a floating gate and a control gate, and the control gate contains a metal or a metal silicide.

37. (Previously Presented) The device according to claim 36, wherein the metal contains tungsten.

38-44. (Canceled)

45. (Currently Amended) A nonvolatile semiconductor memory device, comprising:

a semiconductor substrate having a peripheral circuit region and a memory cell region;

a first element region provided in the ~~peripheral circuit~~ memory cell region;

a second element region provided in the ~~memory cell~~ peripheral circuit region;

~~a first element isolation region provided in the semiconductor substrate, the first element isolation region isolating the first element region;~~

~~a second element isolation region provided in the semiconductor substrate, the second element isolation region isolating the second element region;~~

~~a first transistor~~ a plurality of memory cells and a selection transistor each having source and drain diffusion layers each provided in the first element region;

a ~~second~~ peripheral transistor having source and drain diffusion layers each provided in the second element region; ~~and~~

an element isolation region being in contact with the first element region;

an insulating film covering ~~the first and second transistors and the first and second element isolation regions~~ the plurality of memory cells, the selection transistor, the peripheral transistor, and the element isolation region and containing an insulator different from the element isolation region, the insulating film being harder for an oxidizing agent to pass therethrough, compared with a silicon oxide film, and a surface of the insulating film being oxidized;

an inter-level insulating film provided on the surface of the insulating film, the inter-level insulating film containing an insulator different from the insulating film;

a contact hole provided in the inter-level insulating film and the insulating film, the contact hole reaching at least one of the source and drain diffusion layers of the selection transistor and overlapping the element isolation region; and

a contact plug provided in the contact hole, the contact plug being in contact with at least one of the source and drain diffusion layers of the selection transistor, the insulating film, and the inter-level insulating film.

46-48. (Canceled)

49. (Currently Amended) The device according to claim ~~48~~ 45, wherein a diameter of the contact hole is wider than a width of the ~~second~~ first element region.

50. (Canceled)

51. (Currently Amended): The device according to claim 45, wherein surfaces of gate electrodes of ~~the first and second transistors~~ the memory cells, the selection transistor, and the peripheral transistor are oxidized.

52. (Previously Presented) The device according to claim 45, wherein the insulating film has a thickness of at most 50 nm.

53. (Previously Presented) The device according to claim 45, wherein the insulating film includes a silicon nitride film.

54. (Previously Presented) The device according to claim 53, wherein a surface of the silicon nitride film is oxidized.

55. (Previously Presented) The device according to claim 54, wherein a thickness of an oxidized region of the silicon nitride film is at least 1 nm and at most 10 nm.

56. (Previously Presented) The device according to claim 53, wherein the silicon nitride film contains hydrogen, and a concentration of the hydrogen is at most $3 \times 10^{21}$ atom/cm$^3$.

57. (Previously Presented) The device according to claim 53, wherein the silicon nitride film contains hydrogen, and a concentration of the hydrogen gradually becomes higher from the surface of the silicon nitride film.

58. (Currently Amended): The device according to claim 45, wherein a gate electrode of each of ~~the first and second transistors~~ the memory cells, the selection transistor, and the peripheral transistor contains a metal or a metal silicide.

59. (Previously Presented) The device according to claim 58, wherein the metal contains tungsten.

60. (Currently Amended) The device according to claim 45, wherein a gate electrode of each of ~~the first and second transistors~~ memory cells, the selection transistor, and the peripheral transistor is a stacked gate structure including a floating gate and a control gate, and the control gate contains a metal or a metal silicide.

61. (Previously Presented) The device according to claim 60, wherein the metal contains tungsten.

62-68. (Canceled)

69. (New) The device according to claim 26, wherein a diameter of the contact hole is wider than a width of the first element region.

70. (New) The device according to claim 26, wherein the memory cell constructs a NAND EEPROM.

71. (New) The device according to claim 45, wherein the memory cells construct a NAND EEPROM.